

AMENDMENTS

In the Specification:

Please amend the specification by substituting the following paragraphs:

On Page 3, please amend the heading on line 15 by substituting the following:

a1 DETAILED DESCRIPTION OF THE INVENTION

On Page 3, please amend the Paragraph starting at line 25 and ending at line 28 by substituting the following:

Q2 Sub B1 Figs. 1 and 2 depict elevational section views of the prior art ^{microstrip} strip line 1 and ^{strip line} microstrip monolithic 5 constructions respectively. Both of these constructions are well known in the planar fabrication and microcircuit technology. In Fig. 1, the strip line comprises a metal conductor etched on top of an insulator.

On Page 3, please amend the Paragraph starting at line 30 and ending at Page 4, line 2, by substituting the following:

Q3 Sub B2 The ^{strip} microstrip construction 5 shown in Fig. 2 comprises a pair of metal conductors 6 and 8 in spaced apart positions with one of the conductors 9 embedded within the insulation material 7. In both of these constructions, the only way to achieve field isolation is to space adjacent conductors apart. However, this uses an undesirable amount of surface area on the substrate to achieve such isolation.

On Page 4, please amend the Paragraph starting at line 4 and ending at line 17 by substituting the following:

Referring to Fig. 3, an on-chip three layer metal-shielded monolithic transmission line of the present invention comprises, in a simple embodiment, three parallel planar thin film, conductive layers 10 which are typically one micron thick condensates of Cu, Al, or Au placed by, for example, a physical vapor deposition process such as evaporation or sputtering. Each adjacent pair of the conductive layers 10 is separated by one of a plurality of planar thin film nonconductive separator layers 20, typically an oxide deposited or grown, to form a stack 30 of alternating conductive 10 and nonconductive 20 layers. An initial one 12 and a final one 14 of said conductive layers 10 form a top and a bottom conductive planes, the conductive planes establishing a mutually registered selected width 32 of the stack 30. A center one 16 of the conductive layers 10 comprises three laterally spaced apart conductive strips 16', 16" and 16''' separated laterally by a pair of non conductive spacer layers 40, the two laterally terminal 16' and 16''' of the three conductive strips 16', 16" and 16''' being spaced at approximately the selected width 32.

On Page 4, please amend the paragraph starting at line 31 and ending at Page 5, line 11 by substituting the following:

as Referring to Fig. 4, the above-described configuration may be further extended to include additional layers such as the 5 metal layer embodiment shown. In this further embodiment, the plurality of parallel planar thin film, conductive layers 10 are formed wherein each adjacent pair of the conductive layers is separated by one of the plurality of planar thin film nonconductive separator layers 20 to form the stack of alternating conductive and nonconductive said layers 30. The initial one 12 and final one 14 of conductive layers 10 form the top and bottom conductive planes as before, the conductive planes establishing the mutually registered selected width 32 of the stack. One of the conductive layers 16 between the top and the bottom conductive planes 12, 14, comprises three laterally spaced apart conductive strips 16', 16", 16''' separated by a pair of nonconductive laterally spaced apart spacer layers 40, the two laterally terminal 16', 16" of the three conductive strips being spaced approximately at the selected width 32 as in the previous embodiment.

On Page 6, please amend the paragraph starting at line 31 and ending at Page 7, line 4 by substituting the following:

as shown in Fig. 6, because the vias 22 are generally only able to be fabricated with limited lengths "L", the spaces 24 between adjacent vias 22 of one shield side wall are staggered with respect to the spaces 24 between adjacent vias 22 of the adjacent next side wall so as to provide full isolation between adjacent center conductors 16' and 16" as, for instance, when the constructions defined above are positioned side-by-side on the substrate.

On Page 7, please amend the paragraph starting at line 13 and ending at line 16 by substituting the following:

Q7 SUB BT The process further comprises the step of extending, by simple metal deposition, the initial one 12 and the final one 14 of said ~~conductive~~ layers, as the top and the bottom conductive planes, to define the mutually registered selected width 32 of the stack 30.